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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,945	03/10/2004	Jhon Jhy Liaw	67,200-1253	4848

7590 10/24/2006

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EXAMINER	
ARENA, ANDREW OWENS	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 10/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,945	LIAW, JHON JHY	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-22,24-30 and 32-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-22, 24-30, and 32-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Fig 1E is objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "24B" has been used to designate both an ARC layer directly on top of 24A and an ARC layer directly on top of 24C. Uppermost 24B should be 24D.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance. See MPEP § 608.02(p).

Claim Objections

Claim 18 is objected to because the recitation "each of the first second plurality...form a continuous" (ln 17-21) is confusing and renders the claim indefinite. First, said recitation is grammatically incorrect and should probably read "each of the first and second pluralities...forms". However, said recitation seems to require that each metal filled opening is itself continuous, which is inherent, and probably not what applicant intends to claim. Another interpretation is that "each first plurality forms a continuous contact interconnect structure with each second plurality, said continuous contact interconnect structure having an aspect ratio...". However, this is not supported by applicant's disclosure (Fig 1E) because not every possible permutation of a first with a second in continuous. Applicant should particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 38 is objected to because there is insufficient antecedent basis for the limitation "second metal filled opening...to the first metal filled openings" in the claim. Claim 38 defines only a single first metal filled opening.

Claim 38 is objected to for minor errors. The skipped line (ln 3) should be removed for consistent form in the claims. The recitation "first second" (ln13) seems to be a misprint and should recite "first and second".

Claims 21 and 40 recite a plurality of elements but the listings of elements are not proper Markush groupings. See MPEP § 803.02.

Claims 24 and 42 are objected to because the recitation "the first and second first and second" seems to be a misprint and should simply recite "the first and second".

Claim 41 is objected to because the recitation "first and second...comprise lowermost...layer" is grammatically awkward. It seems applicant intends to claim "the first and the second contact layers each comprise a lowermost...layer".

Appropriate correction of all above-identified issues is required.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 18-22, 24, 25, 27- 30, 32, 33, 35, 37-40, and 42-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karasawa (US 6,720,628) in view of Chen (6,784,096).

Re claim 18, Karasawa discloses (Fig 12) a contact interconnect structure comprising:

a semiconductor substrate (inherent) comprising CMOS devices (Q5; col 4 ln 42) including active contact regions (17; col 5 ln 25);

a first contact layer (90) overlying the active contact regions comprising a first plurality of metal filled openings (80, 82; col 9 ln 58-59) extending through the first contact layer thickness (col 9 ln 54-56, col 10 ln 16-18) to the active contact regions;

a second contact layer (92) overlying the first contact layer comprising a second plurality (Fig 13) of metal filled openings (84; col 11 ln 45-47), each of said second plurality of metal filled openings extending through the second contact layer thickness (col 11 ln 42-45) to a respective one or more of the first plurality of metal filled openings;

wherein, each of the first [and] second pluralit[ies] of metal filled openings form a (electronically) continuous contact interconnect structure having an aspect ratio with respect to a respective contact layer.

Karasawa differs from the claimed invention only in not expressly disclosing the value of the aspect ratio.

Chen discloses a contact interconnect structure having an aspect ratio less than about 4.5 (col 3 ln 29-33).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Chen, the continuous contact interconnect structure of Karasawa have an aspect ratio less than about 4.5 with respect to a respective contact layer; at least to reduce device size.

Re claim 19, Karasawa as modified by Chen above discloses the bottom portion of said contact interconnect structure has a maximum width (inherent) and an aspect ratio of less than about 4.5

Karasawa as modified by Chen differs from the claimed invention only in not expressly disclosing the width of said interconnect structure.

Chen discloses a contact interconnect structure having a maximum width of less than about 70 nanometers (col 3 ln 29-33).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Chen, the bottom portion of said contact interconnect structure of Karasawa has a maximum width of less than about 70 nanometers; at least to reduce device size.

Re claim 20, Karasawa discloses (Fig 12) an overlying metallization layer (third conductive layer, including 72b; col 10 ln 28-37) in electrical communication with the second plurality of metal filled openings (col 10 ln 44 – col 11 ln 29).

Re claim 21, Karasawa does not limit his first and second contact layers to any particular type, therefore the disclosure of Karasawa encompasses all well-known insulator types, including at least comprising silicon nitride.

Re claim 22, Karasawa does not limit his first and second contact layers to any particular type, therefore the disclosure of Karasawa encompasses all well-known insulator types, including at least comprising silicon nitride. A silicon nitride contact layer inherently has a lowermost portion of silicon nitride.

Re claim 24, Karasawa discloses the first and second plurality of metal filled openings comprise conductive material Ti (col 9 ln 56-59, col 11 ln 42-47).

Re claim 25, Karasawa discloses (Fig 12) the active contact regions are gate electrodes (20, 30; col 6 ln 11-17).

Re claim 27, Karasawa discloses the active contact regions comprise a silicide conductive material (col 6 ln 14-17, col 7 ln 50-51), and does not limit his silicide to any particular type, therefore the disclosure of Karasawa encompasses all well-known silicide types, including NiSi.

Re claim 28, Karasawa does not limit his first and second contact layers to any particular type, therefore the disclosure of Karasawa encompasses all well-known insulator types, including at least comprising silicon nitride. A silicon nitride contact layer inherently has an uppermost portion of silicon nitride; which is capable of serving as a hardmask layer.

Re claim 29, Karasawa does not limit his metal filled opening to any particular shape, therefore the disclosure of Karasawa encompasses all well-known metal filled opening shapes, including circular.

Re claim 30, Karasawa discloses (Fig 12) the first and second plurality of metal filled openings are contact holes (80, 82, 84; col 9 ln 54-56, col 11 ln 42-45).

Re claim 32, Karasawa discloses (Fig 12, 13) a contact interconnect structure comprising:

at least first (90) and second (92) stacked contact layers comprising a respective first (80) and second (84) plurality metal filled openings (col 9 ln 58-59, col 11 ln 45-47)

extending through the first and second contact layers (col 9 ln 54-56, col 10 ln 16-18, col 11 ln 42-45) to a contact region (17; col 5 ln 25) comprising an active transistor region (Q5; col 4 ln 42) to form a stacked contact interconnect structure;

wherein, each of the at least first and second plurality of metal filled openings comprise a bottom portion (inherent) having a maximum width and an aspect ratio with respect to a respective contact layer.

Karasawa differs from the claimed invention only in not expressly disclosing either the maximum width or the aspect ratio.

Chen discloses a contact interconnect structure and teaches an opening width of less than about 70 nm and an aspect ratio of less than about 3.3 (col 3 ln 29-33).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Chen, said bottom portions of Karasawa have a maximum width of less than about 70 nanometers and an aspect ratio of less than about 3.3 with respect to a respective contact layer; at least to reduce device size.

Re claim 33, Karasawa differs from the claimed invention only in not expressly disclosing either the maximum width or the aspect ratio.

Chen discloses a contact interconnect structure and teaches an opening width of less than about 50 nm and an aspect ratio of less than about 4.5 (col 3 ln 29-33).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Chen, said bottom portion of Karasawa has a maximum width of less than about 50 nanometers and an aspect ratio of less than about 4.5; at least to reduce device size.

Re claim 35, Karasawa discloses the active transistor region is gate electrodes (20, 30; col 6 ln 11-17).

Re claim 37, Karasawa discloses the overlying conductive regions comprise a metallization layer (col 7 ln 58-67, col 9 ln 30-50).

Re claim 38, Karasawa discloses (Fig 12) a stacked contact interconnect structure for achieving a high aspect ratio comprising:

a semiconductor substrate (inherent) comprising CMOS devices (Q5; col 4 ln 42) including active contact regions (17; col 5 ln 25);

a first contact layer (90) overlying the active contact regions comprising a first metal filled opening (80; col 9 ln 58-59) extending through the first contact layer thickness (col 9 ln 54-56, col 10 ln 16-18) to the active contact regions;

a second contact layer (92) overlying the first contact layer comprising a second metal filled opening (84; col 11 ln 45-47), extending through the second contact layer thickness (col 11 ln 42-45) to the first metal filled opening;

wherein, each of the first [and] second plurality of metal filled openings have about the same width to form a stacked contact interconnect structure having an aspect ratio with respect to a respective contact layer.

Karasawa differs from the claimed invention only in not expressly disclosing the value of the aspect ratio.

Chen discloses a contact interconnect structure having an aspect ratio less than about 4.5 (col 3 ln 29-33).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Chen, the stacked contact interconnect structure of Karasawa have an aspect ratio less than about 4.5 with respect to a respective contact layer; at least to reduce device size.

Re claim 39, Karasawa discloses a bottom portion of said contact interconnect structure (inherent).

Karasawa differs from the claimed invention only in not expressly disclosing either the maximum width or the aspect ratio.

Chen discloses a contact interconnect structure and teaches an opening width of less than about 70 nm and an aspect ratio of less than about 4.5 (col 3 ln 29-33).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Chen, said bottom portions of Karasawa have a maximum width of less than about 70 nanometers and an aspect ratio of less than about 4.5; at least to reduce device size.

Re claim 40, Karasawa does not limit his first and second contact layers to any particular type, therefore the disclosure of Karasawa encompasses all well-known insulator types, including at least comprising silicon nitride.

Re claim 42, Karasawa discloses the first and second plurality of metal filled openings comprise conductive material Ti (col 9 ln 56-59, col 11 ln 42-47).

Re claim 43, Karasawa discloses the active contact regions are gate electrodes (20, 30; col 6 ln 11-17).

Re claim 44, Karasawa discloses the active contact regions comprise a silicide conductive material (col 6 ln 14-17, col 7 ln 50-51), and does not limit his silicide to any particular type, therefore the disclosure of Karasawa encompasses all well-known silicide types, including NiSi.

Claims 26 and 36 are rejected under 35 USC 103(a) as being unpatentable over Karasawa and Chen as applied respectively to claims 25 and 35 above, and further in view of Ono (IEEE Transactions on Electron Devices, V.42, N.10, Oct. 1995, pg.1822).

Re claims 26 and 36, Karasawa as modified by Chen differs from the claimed invention only in not disclosing a gate length of less than about 45 nm.

Ono discloses a MOSFET (Fig 2a) with a gate structure having a gate length of less than about 45 nm (caption).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Ono, the gate electrode of Karasawa comprises a gate length of less than about 45 nm, at least to reduce device size.

Claims 34 and 41 are rejected under 35 USC 103(a) as being unpatentable over Karasawa and Chen as applied respectively to claims 32 and 36 above, and further in view of Zhou (US 6,358,842).

Re claim 34, Karasawa differs from the claimed invention only in not disclosing the first and second contact layers comprise an underlying etch stop layer.

Zhou discloses (Fig 13) first (62) and second (70) contact layers, each comprising an underlying (58, 66) etch stop layer (either layer can be SiN: col 4 ln 13-14, col 4 ln 60-61; which is capable of serving as an etch stop layer).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Karasawa in view of Zhou such that the first and second contact layers comprise an underlying etch stop layer; at least for etch selectivity.

Re claim 41, Karasawa differs from the claimed invention only in not disclosing the first and second contact layers comprise a lowermost etch stop layer.

Zhou discloses (Fig 13) first (62) and second (70) contact layers, each comprising a lowermost (58, 66) etch stop layer of silicon nitride (col 4 ln 13-14, col 4 ln 60-61; which is capable of serving as an etch stop layer).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Karasawa in view of Zhou such that the first and second contact layers comprise a lowermost etch stop layer of silicon nitride; at least for etch selectivity.

Response to Arguments

Applicant's arguments filed 04/22/2006 have been fully considered but they are not persuasive.

Applicant's arguments that Karasawa fails to disclose "extending through...to a respective one or more of the first plurality" and "form a continuously connected contact interconnect structure" are not persuasive. Applicant has presented neither claim language nor evidence to structurally distinguish said claimed aspects from the corresponding features of Karasawa which examiner has relied upon for rejection. In particular, the language "extending...to" and "continuously connected" must be given their broadest reasonable interpretations. See MPEP § 904.01 and MPEP § 2111.

In response to applicant's arguments against the references individually ("Zhou nowhere discloses...to active contact regions"), one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant's observation that "Chen discloses a method of forming a barrier layer" does not change that Chen discloses the claimed via widths and aspect ratios and suggests including said dimensions in analogous devices (col 1 ln 50-55).

Examiner has established a *prima facie* case of obviousness consistent with all basic requirements. See MPEP § 2143. Applicant has not submitted persuasive evidence of nonobviousness, in particular, that one of ordinary skill would not have been motivated to make examiner's proposed combination.. See MPEP § 2142 (¶1).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is 571-272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on 571- 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Andrew O Arena
19 October 2006

Douglas W. Owens 10/23/06

DOUGLAS W. OWENS
PRIMARY EXAMINER